Kindly **add** the following claims:

--151. A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to a transition of an external clock signal;

receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, wherein the second operation code initiates a read operation in the memory device; and

storing the binary value in the programmable register in response to the first operation code.

152. The method of claim 151 wherein the first operation code is included in a control register access request packet.

153. The method of claim 152 wherein the first operation code and the binary value are included in the same control register access request packet.

154. The method of claim 151 wherein the delay time is representative of a number of clock cycles of the external clock signal to transpire.

155. The method of claim 154 further including:

receiving the second operation code; and

outputting the data, in response to the second operation code, after the number of clock cycles of the external clock signal transpire.

156. The method of claim 155 further including receiving address information synchronously with respect to the external clock signal.

157. The method of claim 156 wherein the address information and the second operation code are included in a read request packet.

158. The method of claim 151 further including:

receiving block size information wherein the block size information is representative of an amount of data to be output;

receiving the second operation code; and

outputting the amount of data in response to the second operation code, after delay time transpires.

159. The method of claim 158 wherein the block size information further defines an amount of data to be input in response to a third operation code, wherein the third operation code initiates a write operation in the memory device, the method further including:

receiving the third operation code; and

inputting the amount of data in response to the third operation code.

160. The method of claim 159 wherein the third operation code is included in a request packet.

161. The method of claim 160 wherein the block size information and the third operation code are included in the same request packet.

162. The method of claim 155 wherein data is output synchronously with respect to consecutive rising and falling edge transitions of the external clock signal.

163. The method of claim 151 wherein the first operation code is received in an initialization sequence after power is applied to the memory device.

164. A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

165. The method of claim 164 wherein the binary value is representative of a number of clock cycles of an external clock signal

to transpire before the memory device outputs data in response to a second operation code.

166. The method of claim 165 further including:

issuing the second operation code to the memory device; and

receiving data output by the memory device after the number of clock cycles of the external clock signal transpire.

167. The method of claim 166 further including providing address information synchronously with respect to the external clock signal.

168. The method of claim 167 wherein the address information and the second operation code are included in a request packet.

169. The method of claim 164 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device in response to the second operation code; and

receiving the amount of data output by the memory device.

170. The method of claim 169 wherein the block size information further defines an amount of data to be input by the memory device in response to a third operation code, the method further including:

issuing the third operation code to the memory device; and

providing the amount of data to the memory device.

171. The method of claim 164 wherein the first operation code and the binary value are included in a request packet.

172. The method of claim 164 wherein the first operation code and the binary value are included in the same request packet.

173. A synchronous memory device including an array of memory cells and at least one programmable register, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

174. The memory device of claim 173 wherein the binary value is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data in response to a second operation code.

175. The memory device of claim 174 further including output driver circuitry to output the data after the number of clock cycles of the external clock signal transpire in response to the second operation code.

176. The memory device of claim 175 wherein the output driver circuitry outputs a first portion of data synchronously with respect to a rising edge transition of the external clock signal and a second portion of data synchronously with respect to a falling edge transition of the external clock signal.

177. The memory device of claim 173 wherein the first operation code is included in a request packet.

178. The memory device of claim 173 wherein the first operation code and the binary value are included in a request packet.

179. The memory device of claim 173 wherein the first operation code and the binary value are included in the same request packet.

180. The memory device of claim 173 wherein the input receiver circuitry is operative to receive a third operation code, wherein the third operation code initiates a write operation in the memory device, and wherein the memory device further includes:

input circuitry to input data in response to the third operation code.--